CLAIM AMENDMENTS

1. (Currently Amended) A method comprising:

amplifying data signals received from a memory bus;

sampling the amplified data signals; and

selectively disabling the amplification in response to the absence of a predetermined operation occurring over the memory bus.

2. (Currently Amended) The method of claim 1, wherein the selectively disabling the amplification comprises:

selectively disabling sense amplifiers.

3. (Currently Amended) The method of claim 1, wherein the selectively disabling the amplification comprises:

selectively disabling the amplification in response to the end of a particular predetermined operation.

4. (Currently Amended) The method of claim 1, further comprising:

reading a data strobe signal from the bus;

delaying the data strobe signal; and

synchronizing the ~~disablement~~ disabling of the amplification to an edge of the delayed data strobe signal.

5. (Original) The method of claim 1, further comprising:

communicating signals associated with a double data rate memory device over the memory bus.

6. (Original) The method of claim 1, wherein the predetermined operation comprises a read operation.

7. (Original) The method of claim 1, wherein the predetermined operation comprises a write operation.

8. (Currently Amended) A method comprising:

amplifying data signals received from a memory bus;

sampling the amplified data signals; and

selectively enabling the amplification in response to a predetermined operation occurring over the memory bus.

A14

9. (Currently Amended) The method of claim 8, wherein the selectively enabling the amplification comprises:

selectively enabling sense amplifiers.

10. (Currently Amended) The method of claim 8, wherein the selectively enabling the amplification comprises:

selectively enabling the amplification in response to the beginning of the predetermined operation.

11. (Currently Amended) The method of claim 8, further comprising:

synchronizing the ~~enablement~~ enabling of the amplification to the edge of a data strobe signal that appears on the memory bus in connection with the predetermined operation.

12. (Original) The method of claim 8, further comprising:

communicating signals associated with a double data rate memory device over the memory bus.

13. (Original) The method of claim 8, wherein the predetermined operation comprises a read operation.

14. (Original) The method of claim 8, wherein the predetermined operation comprises a write operation.

15. (Original) An apparatus comprising:

amplifiers to amplify data signals received from a memory bus;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to selectively disable the amplifiers in response to the absence of a predetermined operation occurring over the memory bus.

16. (Original) The apparatus of claim 15, wherein the second circuit selectively disables the amplifiers in response to the end of a particular read operation.

A 14

17. (Original) The apparatus of claim 15, wherein the predetermined operation comprises a read operation.

18. (Original) The apparatus of claim 15, wherein the predetermined operation comprises a write operation.

19. (Original) The apparatus of claim 15, wherein the apparatus comprises a memory controller.

20. (Original) The apparatus of claim 15, wherein the apparatus comprises a memory device.

21. (Currently Amended) An apparatus comprising:

amplifiers to amplify data signals received from a memory bus;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to selectively enable the amplifiers in response to ~~the~~ a beginning of a predetermined operation occurring over the memory bus.

22. (Original) The apparatus of claim 21, wherein the second circuit selectively disables the amplifiers in response to the end of a particular read operation.

23. (Original) The apparatus of claim 21, wherein the predetermined operation comprises a read operation.

24. (Original) The apparatus of claim 21, wherein the predetermined operation comprises a write operation.

25. (Original) The apparatus of claim 21, wherein the apparatus comprises a memory controller.

26. (Original) The apparatus of claim 21, wherein the apparatus comprises a memory device.

27. (Original) A computer system comprising:

a memory;

a memory bus coupled to the memory;

a processor to initiate a predetermined operation with the memory over the memory bus;

amplifiers to amplify data signals received from the memory bus;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to selectively disable the amplifiers in response to the absence of the predetermined operation occurring over the memory bus.

28. (Original) The computer system of claim 27, wherein the predetermined operation comprises one of a read operation and a write operation.

29. (Currently Amended) A computer system comprising:

a memory;

a memory bus coupled to the memory;

a processor to initiate a ~~predefined~~ predetermined operation with the memory over the memory bus;

A 14

amplifiers to amplify data signals received from the memory bus;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to selectively enable the amplifiers in response to the beginning of the predetermined operation occurring over the memory bus.

30. (Original) The computer system of claim 29, wherein the predetermined operation comprises one of a read operation and a write operation.